

AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) A processor comprising:

a queue configured to store one or more instructions to be issued; and

a control circuit coupled to the queue, wherein the control circuit is configured to detect a replay of a ~~first~~ an instruction due to a ~~dependency on~~ a load miss, and wherein the control circuit is configured to enter into a stall state and inhibit issuance of the one or more instructions in the queue to one or more pipelines of the processor responsive to detecting the replay until fill data in response to the load miss is being returned for loading, the control circuit further includes a storage device to store a miss tag corresponding to the load miss and to compare the stored miss tag to a fill tag that is sent to the control circuit when fill data is returned, in which when the miss tag and the fill tag match, the control circuit to exit the stall state to start issuing instructions from the queue.

2. (currently amended) The processor as recited in claim 1 wherein the control circuit is configured to inhibit issuance of the ~~one or more~~ instructions until fill data is provided to a data cache of the processor.

3. (canceled)

4. (currently amended) The processor as recited in claim ~~3~~ 2 wherein the control circuit further includes a storage device, and wherein the control circuit is configured to read a miss tag from a read queue that stores one or more load misses, the miss tag identifying the load miss on which the first instruction is dependent, and wherein the control circuit is configured to store the miss tag in the storage device, and wherein the control circuit further includes a comparator coupled to the storage device and coupled to receive a fill tag identifying fill data being provided to the data cache, and wherein the comparator is configured to compare the miss tag stored therein to the fill tag to determine if the fill

data being returned corresponds to the load miss.

5. (currently amended) The processor as recited in claim 2 wherein ~~the fill data corresponds to any load miss~~ multiple load misses may be present in which comparison of the miss tag and the fill tag identifies fill data to its corresponding load miss.

6-9. (canceled)

10. (currently amended) The processor as recited in claim ~~6~~ 2 wherein the control circuit is configured to permit issuance of one of the one or more instructions if one or more ~~issue criteria are fulfilled for that instruction~~ instructions lack dependency to the load miss.

11. (currently amended) The processor as recited in claim 10 wherein ~~the one or more issue criteria includes a lack of dependencies being detected for that instruction in~~ to the load miss are maintained by one or more scoreboards coupled to the control circuit.

12. (currently amended) The processor as recited in claim ~~4~~ 11 wherein the control circuit is configured to detect ~~the dependency of the first instruction~~ dependencies on the load miss using one or more scoreboards which track instructions that have passed a first stage of the one or more pipelines a pipeline, wherein the first stage is the stage at which where replay is signaled.

13. (canceled)

14. (currently amended) A method comprising:

detecting a replay of a first instruction due to a dependency on a load miss; ~~and~~

inhibiting issuance of one or more instructions from a queue to ~~one or more pipelines of the~~ a pipeline of a processor responsive to detecting the replay by entering a stall state;

storing a miss tag corresponding to the load miss in response to detecting the replay;

generating a fill tag when fill data corresponding to the load miss is returned

comparing the fill tag to the miss tag to identify when fill data corresponding to the load miss is being returned; and

exiting the stall state to allow one or more instructions to issue after comparing the fill tag and the miss tag results in a match.

15. (currently amended) The method as recited in claim 14 ~~further comprising inhibiting issuance of the~~ wherein exiting the stall state to allow one or more instructions until to issue occurs after fill data is provided to a data cache.

16. (canceled)

17. (currently amended) The method as recited in claim ~~16~~ 15 further comprising: ~~reading a~~ the miss tag from a read queue that stores one or more load misses, wherein the miss tag identifies the load miss ~~on which the first instruction is dependent; and~~
 ~~comparing the miss tag to a fill tag identifying the fill data to determine if the fill data corresponds to the load miss.~~

18. (currently amended) The method as recited in claim 15 ~~wherein the fill data corresponds to any load miss~~ multiple load misses may be present in which comparing the miss tag and the fill tag identifies fill data to its corresponding load miss.

19-22. (canceled)

23. (currently amended) The method as recited in claim ~~19~~ 15 further comprising permitting issuance of one of the one or more instructions ~~is responsive to if one or more issue criteria being fulfilled for that instruction~~ instructions lack the dependency to the load miss.

24. (currently amended) The method as recited in claim 23 ~~wherein the one or more issue criteria includes~~ further comprising detecting a lack of dependencies dependency ~~for that~~ an instruction in one or more scoreboards.

25. (currently amended) The method as recited in claim ~~14~~ 23 ~~wherein the~~ further comprising detecting the lack of dependency for an instruction ~~comprises by checking~~ one or more scoreboards which track instructions that have passed a first stage of the ~~one or more pipelines, wherein the first stage is the stage at which~~ pipeline where replay is signaled.

26. (canceled)

27. (currently amended) A ~~more earlier~~ computer accessible medium comprising one or more data structures ~~representing to manufacture a processor, the processor~~ including:

a queue configured to store one or more instructions to be issued; and

a control circuit coupled to the queue, wherein the control circuit is configured to detect a replay of a ~~first~~ an instruction due to a ~~dependency on~~ a load miss, and wherein the control circuit is configured to enter into a stall state and inhibit issuance of the one or more instructions in the queue to one or more pipelines of the processor responsive to detecting the replay until fill data in response to the load miss is being returned for loading, the control circuit further includes a storage device to store a miss tag corresponding to the load miss and to compare the stored miss tag to a fill tag that is sent to the control circuit when fill data is returned, in which when the miss tag and the fill tag match, the control circuit to exit the stall state to start issuing instructions from the queue.